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| 09/880,749 | 06/12/2001 | Andrew M. Draper | 015114-053600US | 5820 |

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| EXAMINER | |
|---|---|
| KERVEROS, JAMES C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | 8 |

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/880,749 | Applicant(s) DRAPER, ANDREW M. | |
|---|---|---|---|
| | Examiner James C Kerveros | Art Unit 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This is a Non-Final Office Action in response to Amendment filed March 30, 2004.

Claims 1-29 are pending and are presently being under examination.

Claim Objections, in the Prior Office Action, is hereby withdrawn in view of the corrections made by the amendment.

### *Drawings*

2. The drawings are objected to because this application lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-26, 28 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: The structural limitation for a "***programmable logic portion"*** recited in claims 1, 11, 21 and 28 lacks a structural cooperative relationship with the proceeding limitations for "a first and a second JTAG circuit".

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 27 is rejected under 35 U.S.C. 102(e) as being anticipated by Au et al. (US 6681359).

Regarding independent Claim 27, Au discloses an integrated circuit (100, FIG. 3), comprising:

A processor comprising a first JTAG circuit including a Memory Built-In Self-Test (MBIST) (116) using a JTAG-compliant interface and a JTAG Test Access Port controller coupled to the instruction and plurality of data registers (34, 36) and boundary scan data registers (24, 26) in FIG. 1, which shows a JTAG-compliant integrated circuit, illustrating the relationship between the core logic, input/output pins, the scan elements arranged within the integrated circuit, and a TAP controller.

A second JTAG circuit, which is the exact identical mirror image of the first JTAG circuit described above. The second JTAG circuit with the MBIST located in the lower

left corner of IC 100 is coupled to the first JTAG circuit with the MBIST located in the upper left corner of IC 100, and also is coupled to the processor (132).

Au, further, discloses a first instruction and plurality of data registers (34, 36) and boundary scan data registers (24, 26) in the MBIST located in the upper left corner of IC 100, and a second instruction and first plurality of data registers (34, 36) and boundary scan data registers (24, 26) in the MBIST located in the lower left corner of IC 100, wherein the first registers are designed to perform functions that are not performed by the second registers, since they are both functionally independent from each other because they are located in different MBIST circuitry independent of ach other.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-26, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al. (US 6681359).

Regarding independent Claims 1, 11, 21, Au substantially discloses an integrated circuit (100, FIG. 3), comprising:

A first JTAG circuit including a Memory Built-In Self-Test (MBIST) (116) using a JTAG-compliant interface and a JTAG Test Access Port controller coupled to the instruction and plurality of data registers (34, 36) and boundary scan data registers (24, 26), in FIG. 1, which shows a JTAG-compliant integrated circuit, illustrating the relationship between the core logic, input/output pins, the scan elements arranged within the integrated circuit, and a TAP controller.

An embedded portion part which is inherent in the integrated circuit (100), including a processor (diagnostic block 132) and a second JTAG circuit, which is the exact identical mirror image of the first JTAG circuit described above. The second JTAG circuit with the MBIST located in the lower left corner of IC 100 is coupled to the first JTAG circuit with the MBIST located in the upper left corner of IC 100, and also is coupled to the processor (132).

Regarding independent Claims 1, 11, 21, Au does not explicitly disclose a "programmable logic portion" in an integrated circuit. However, Au discloses a memory matrix (136), where a portion of the memory matrix interfaces with an MBIST for being tested over a bi-directional bus (138) in the IC 100. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a programmable logic portion in the integrated circuit (100) of Au, since the MBIST disclosed by Au is capable of testing a programmable logic, using a JTAG-compliant interface.

Regarding Claims 2, 3, 14, 15, 23 and 28, Au does not explicitly disclose a "programmable logic portion", where a data register is used to load data into the

programmable logic portion to configure logic circuitry in the programmable logic portion, and wherein a data register allows a user to transmit and receive data from the programmable logic portion on input/output pins. However, Au discloses a memory matrix (136), where a portion of the memory matrix interfaces with an MBIST for being tested over a bi-directional bus (138) in the IC 100. He further discloses instruction and plurality of data registers (34, 36) and boundary scan data registers (24, 26) located in the MBIST, which communicate with the memory matrix (136) over the bi-directional bus (138). The data register allows a user to transmit and receive data from the memory matrix (136) over the bi-directional bus, such as data corresponding to "Test Data Out" (TDO) (18, FIG. 1), data (80, FIG. 2) and TDI (Test Data In) 102, FIG. 3. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a programmable logic portion in the integrated circuit (100) of Au, since the MBIST disclosed by Au is capable of testing a programmable logic by transmitting and receiving test data from a data register to the memory matrix as indicated above, using a JTAG-compliant interface.

Regarding Claim 4-7, 16-18, Au discloses boundary scan data registers (24, 26) for communicating between the embedded logic portion part of integrated circuit (100) and an external host processor such as a microprocessor, which is part of an external tester linked to a single JTAG interface through TAP controller (112, FIG. 3, also see col.7, lines 15-25).

Regarding Claim 8, Au discloses a first plurality of data registers such as boundary scan data registers (24, 26) corresponding to the MBIST located in the upper

left corner of IC 100, and a second plurality of data registers (34, 36) such as boundary scan data registers (24, 26) corresponding to MBIST located in the lower left corner of IC 100, wherein the second plurality of data registers (24, 26) are disabled through (MUX 32, FIG. 1) by deselecting (26) output, when one of the first plurality of data registers is enabled.

Regarding Claims 9, 10, 19, 20, 25, 26, Au discloses data registers (24, 26) coupled to multiplexer (MUX 32, FIG. 1) of first JTAG circuit controlled by the instruction register (34), where the test data output (TDO) connected to (TDI) input from the first JTAG test circuit and are coupled to multiplexer (MUX 32, FIG. 1) controlled by the TAP controller of the second JTAG test circuit.

Regarding Claims 12, 13, Au discloses a second JTAG circuit comprising a second plurality of data registers (24, 26) coupled to a second TAP controller 38, FIG. 1, wherein one of the second plurality of data registers comprises a bypass register (30) that allows the signals entering TDI 16 to pass directly to TDO 18, via MUX 32, without having to be sequentially shifted through scan cells data registers (24 and 26). A second plurality of data registers coupled to a second TAP controller 38, wherein one of the second plurality of data registers comprises a data register (24, 26) that can force data onto and capture data from a plurality of input/output pins (12, 14).

Regarding Claim 22, Au discloses a first and second JTAG circuits comprising first and second TAP controllers (38, FIG. 1), respectively.

Regarding Claim 29, Au discloses a second JTAG circuit comprising MUX 32, having a first input (TDI) coupled to an output (TDO) of the first JTAG circuit and a

second input coupled to register (26) output to receive data signals from one of the second plurality of data registers (24, 26).

***Response to Arguments***

6. Applicant's arguments filed March 30, 2004 have been fully considered but they are not persuasive. Claims 1-26, 28 and 29 are rejected under 35 U.S.C. 112, second paragraph, Claim 27 is rejected as being anticipated by Au et al., and Claims 1-26, 28 and 29 are rejected as being unpatentable over Au et al. (US 6681359).

In reference to the 112, second paragraph rejection regarding the structural limitation of "***programmable logic portion"*** for lacking a structural cooperative relationship, the applicant argues, page 8, that "the specification of the present application does not state that the programmable logic portion is an essential element of all embodiments of the invention". In response to applicant's argument, the Examiner motes that the structural feature of a "programmable logic portion" is a critical element in relation with the other features recited in an independent claim, for the purpose of understanding and making use of the Applicant' invention. An independent claim must be able to stand alone, without having to refer to other dependent claims for clarity. If the Applicant still contends that the limitation is not critical feature for the Applicant's invention, then such limitation should be removed from the claimed invention.

Applicant's arguments with respect to the prior art rejection with respect to claims 1-29, page 9, have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 6 May 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100